



**Warpage Control for Ultra-Large Packages**: Chip-on-wafer-on-substrate (CoWoS) technology is a 2.5D/3D platform used to integrate SoC (system-on-a-chip) and HBM (high-bandwidth memory) dies on an interposer. As the requirements of AI and high-performance computing push the limits of bandwidth and performance, the sizes of both the integrated dies and the interposers have been increasing. That means warpage control is becoming an urgent challenge, because it impacts joint quality, assembly yields, functional testing and board-level assembly. TSMC’s CoWoS-R platform uses an organic polymer-based interposer that incorporates a redistribution layer (RDL). At ECTC, TSMC researchers will report on their studies of warpage in ultra-large (110x110mm2) CoWoS-R interposers which integrate 4 SoCs and 12 HBMs. They will present the results of their analyses, which took into account substrate size, CoW effects, stress buffering films, heat sink placement and others, and will identify remaining critical challenges going forward.

**Above**: As interposer sizes becomes larger, a key consideration is how surface topography might impact the mounting of SoCs and HBMs on the interposer. The images above show:

1. the microbump is well is joined as the RDL was increased 9 layers
2. measured wafer surface topography shows variation of no more than 7µm across the wafer surface

**(Paper 4.2, “*Package Warpage Reduction for Large CoWoS-R Packages*,” Yu-Hsiang et al, TSMC)**